Review of State-of-the-Art Integration Technologies in Power Electronic Systems

Kangping Wang, Zhiyuan Qi, Fei Li, Laili Wang, and Xu Yang

***Abstract*—As an important development direction of power electronic systems, the integration technologies can bring many benefits, such as size reduction, reliability improvement, cost saving and so on. With the continuous development of power semiconductor devices, especially the emergence of wide band-gap devices, more advanced integration technologies are needed. This paper reviews the state-of-art integration technologies, including active and passive integration technologies. Active integration technology is reviewed in terms of the interconnect, packaging material, packaging structure, and module integration. Passive integration technology is reviewed from the aspects of magnetic integration technology, electromagnetic integration technology, and low-temperature cofired ceramic (LTCC) technology. Higher-level integration technologies, namely power supply on chip (PwrSoC) and power supply in package (PwrSiP), are also investigated, which are mainly used in low power applications.**

***Index Terms*—Active integration, power electronic integration technology, passive integration, power module, wide band-gap device.**

I. Introduction

POWER electronics integration is a technology that integrates multiple power electronic components into a single module, which can offer many benefits such as size reduction, costs saving, and reliability improvement. In recent years, the power electronics integration technology has attracted more and more attentions, especially with the emergence of wide bandgap devices. According to device characteristics and manufacturing process, the power electronics integration technologies can be mainly classified into active integration technology and passive integration technology.

The integration of active components into a module, i.e. active integration technology, can realize low parasitics, good thermal performance, high reliability, etc. In most of available commercial power modules, the interconnections are realized by wire-bonding technology [1]-[5], shown in Fig. 1. However, this traditional packaging structure is not suitable for wide band-gap (WBG) devices which can operate at much higher frequency and temperature than Si devices [6]-[8].

Manuscript received December 5, 2018. This work was supported in part by the Young Scientists Fund of the National Natural Science Foundation of China under Grant 51607141.

The authors are with the State Key Laboratory of Electrical Insulation and Power Equipment, Xi'an Jiaotong University, No.28 Xianning West Road, Xi'an, Shaanxi, 710049, China (e-mail: wangkangping@stu.xjtu.edu.cn; mambaqizhy@stu.xjtu.edu.cn; lifeihelen@stu.xjtu.edu.cn; llwang@xjtu.edu.cn; yangxu@mail.xjtu.edu.cn).

Digital Object Identifier 10.24295/CPSSTPEA.2017.00027

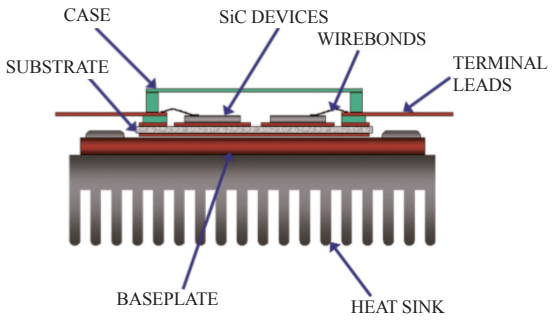


Fig. 1. Conventional wire-bonding power module structure [37].

This is because wire-bonding structure has large parasitic inductance (usually more than 10 nH) and limited heat dissipation capability [5], [9]. Besides, the lead-solder in die attachment has some drawbacks, such as low thermal conductivity, low melting point, and contamination to environment [10]-[12]. So advanced active packaging technologies involving wirebond-less interconnection technology [5], [13]-[21], advanced packaging materials [10], [22]-[26], advanced packaging structures [27]-[34] and module integration technologies [35], [36] are required to be developed.

The passive components, namely inductors, capacitors and transformers, generally occupy a large space of the total volume, which is harmful to the miniaturization of power converters. The passive integration technology, which is to integrate multiple passive components into a single module, has considerably advantages, such as size reduction and cost saving. The magnetic integration is to integrate the inductors and transformers into a single core, which has been successfully applied in some topologies, such as Cuk converter [38], forward converter [39], current-doubler rectifier [40], multiphase converter [41] and LLC converter [42], [43]. The integration of the capacitors and the magnetic components, namely the electromagnetic integration, can further reduce the number and size of the passive components. It has been implemented into LLC converters and asymmetrical half bridge circuit with current-doubler rectifier [44]. Moreover, the integration of all the components of a converter, including passive components, switches, drivers, and controllers, as a module or chip, can achieve greater improvement. Two typical examples are power supply on chip (PwrSoC) and power supply in package (PwrSiP). In recent years, the low-temperature cofired ceramic (LTCC) magnetics have gained much attentions in the 3D integration modules due to its low profile and flexible structure.

In order to break through the bottleneck of integration technologies for further improving the performance of power

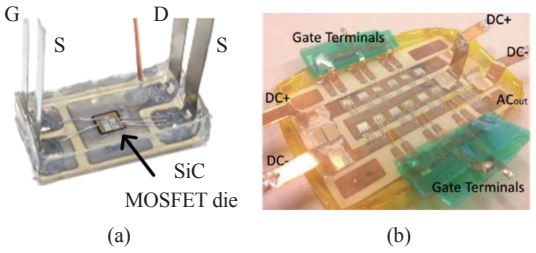


Fig. 2. Improved wire bonding based on (a) Lead frame structure [46], (b) Double-ended-sourced structure [47].

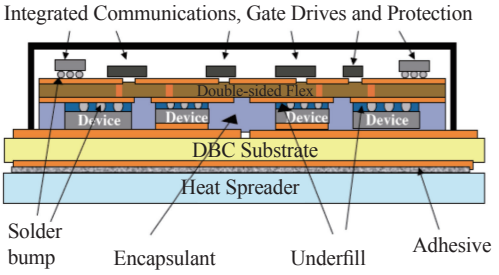


Fig. 3. Flip-Chip based module structure [20].

converters [45], this paper provides a review of the integration technologies from the aspects of active packaging integration and passive integration. Section II reviews the active integration technologies, including interconnection technology, packaging material technology, packaging structure technology, and module integration technology. Section III reviews the passive integration technologies, including the magnetic integration technology, electromagnetic integration technology, PwrSoC and PwrSiP technology, and LTCC integration technology. Section IV concludes the paper.

II. Active Integration Technologies

The integration of active devices can reduce the interconnection parasitic inductance, improve the thermal dissipation capability, reduce the cost, etc. The emergence of wide bandgap devices, such as SiC and GaN, puts higher demands on the active integration. This section will review the active integration technologies from the aspects of interconnection technology, packaging materials, advanced packaging structures, and module-level integration.

A. Interconnection Technology

The interconnection technology is to realize the connection of die to die, and die to external terminals or circuits, which is an indispensable part of packaging technology. The traditional interconnection is based on wire-bonding technology, which has large parasitic inductance, limited heat-dissipation capability and low reliability, etc. Advanced interconnection technologies, including improved wire-bonding interconnections and wirebond-less interconnections, have been developed.

1) Improved Wire-Bonding Interconnection

To utilize the advantages (such as easy realization and low cost) of conventional wire-bonding technology, advanced wire-bonding technology has been developed. In Fig. 2(a), by employing a 3D lead-frame structure, the symmetrical Kelvin Source connection for each switching device was enhanced, which can realize reduced parasitic inductance [46]. In [47], a "double-ended-sourced" busbar structure in the multi-chip module was used to realize symmetrical power loop, thus the circulating current was reduced and dynamic current was balanced, shown in Fig. 2(b). However, the power loop in these improved wirebond-less structures are still a lateral structure. In [48]-[50], a hybrid packaging structure with multilayer substrates are utilized to realize the vertical power loop with small parastics.

2) Wirebond-Less Interconnection

So far, several wirebond-less technologies have been put forward, including flip-chip technology, dimple array interconnection technology, embedded packaging technology, metal-post interconnection technology, etc.

a) Flip-Chip Technology

At the beginning, the flip-chip technology was widely used in the field of microelectronics integration, due to its low-cost, high density, and reliable interconnections [5]. This technology eliminates the wire-bonds by utilizing solder joints for interconnecting devices. Compared to conventional wire bonding package structure, flip-chip structure has reduced parasitics and improved reliability. Owing to these benefits, it is extended to power electronics applications. A flip-chip on flex (FCOF) integrated power electronics module (see Fig. 3) was proposed by John G. Bai, *et al*. in 2003 [19]. In the module, the power chips are flip-soldered on a double-sided flexible copper-clad laminate. For better thermal performance, the power chips are also soldered onto a patterned direct bond copper (DBC) substrate. Between the flex substrate and DBC substrate, an organic underfill material is filled to achieve encapsulation, which can help to reduce thermal stress and improve heat dissipation. However, this technology cannot carry large current and is not suitable for vertical power devices. This technology is expected to be used in lateral GaN modules.

b) Dimple Array Interconnection Technology

With the purpose of enhancing thermal reliability of the solder bump, Simon S. Wen developed the dimple array interconnect (DAI) technique in 2001 [14], [18], [20]. As shown in Fig. 4, the copper flex with pre-formed dimples are used to replace wire bonds as electrical interconnections. The dimpled metal interconnects enable easy forming of solder joints with the underlying devices. Smooth fillets in solder bumps can be formed to significantly reduce the thermal stresses and strains.

The solder joint always forms an hourglass-shape in the DAI processing, which suffers a very small inelastic strain during thermal cycling. Furthermore, DAI provides better thermal management, due to its simpler thermal interfaces, shorter heat dissipation path through the interconnects [14]. However, it requires a special equipment to produce and install the

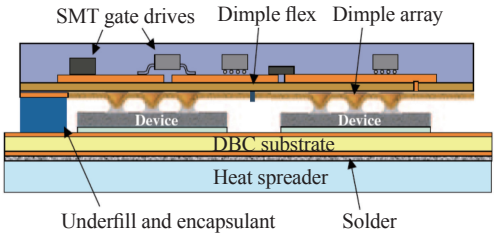


Fig. 4. DAI based module structure [20].

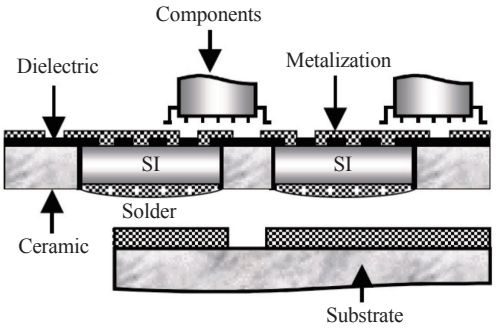


Fig. 5. Embedded power module structure [20].

copper sheet with dimple array.

c) Embedded Packaging Technology

Fig. 5 shows the conceptual embedded power packaging structure. In the structure, the embedded power devices are mounted in the openings etched out of the ceramic frame, and surrounded by an adhesive polymer. After a dielectric layer is coated on the upper surface of ceramic and power chips, via hole through the dielectric is formed on the die pad. And then the interconnections are realized by metallization on surface of the insulation layer [5], [13], [15]-[17]. The base substrate provides electrical interconnection and thermal dissipation path of power chips. This structure can realize reduced parasitics, improved power density, and low mechanical stress.

d) Metal-Post Interconnection Technology

The metal posts interconnected parallel plate structure (MPIPPS) was proposed to achieve interconnections by metal posts in [16], [18]. As shown in Fig. 6, the power chips are sandwiched between two substrates. The bottom of device is attached to the bottom plate by conventional solder die-attach processes, whereas the topside's connection to the top plane is realized through an array of metal posts. Through elimination of the wire-bonds, this technology can reduce the parasitic inductance of the interconnections.

Furthermore, MPIPPS can improve the heat dissipation capability of package due to the two directional heat transfer paths through the substrate and metal post. In addition, active heat dissipation can be implemented by filling the solid or liquid insulating thermal conductive materials in the space between parallel plates and the metal posts. In [21], the experimental results show that the maximum junction temperature of the IGBT chips in the MIPPS module is 17 °C lower than that in wire-bonding module.

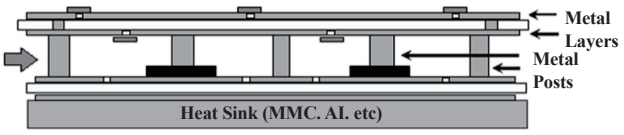


Fig. 6. MPIPPS module structure [21].

B. Packaging Material Technology

The state-of-the-art commercial power devices only can operate up to 175 ºC, which is mainly limited by packaging materials besides packaging structure. To enable WBG devices operating at high temperatures (200–350 ºC), advanced packaging materials are required to provide compatible CTE with WBG chips, and reliable high temperature performance [37]. It is essential to conduct a review of the packaging materials, which mainly include substrate materials, die-attaching materials, and encapsulation materials.

1) Substrate Materials

The substrate provides cooling, interconnection, and mechanical support for the power modules. The commonly used substrates are DBC ceramic substrate and insulating metal substrate (IMS).

In DBC ceramic substrates, Al_2O_3, AlN, BeO and Si_3N_4 can be used as the insulating materials [51]. Though BeO has the highest thermal conductive performance, it is not commonly used because the particle generated during the processing is harmful to human health. The Si_3N_4 material is also not commonly used for its low thermal conductivity and high material cost. Because the strong adhesion of substrate and copper can be easily achieved, Al_2O_3 is the most commonly used insulating materials. Compared with Al_2O_3, AlN has much higher thermal conductivity and closer CTE to SiC, but the AlN DBC substrate is costlier due to more complicated manufacturing process. With the development of manufacturing technique, AlN has the potential to replace Al_2O_3.

Generally, IMS consists of a highly thermal-conductive insulating resin sheet, a copper baseplate and thick copper foils, which can achieve good heat dissipation, and is cheaper than DBC due to the relatively simpler fabrications. IMS has been successfully applied to Mitsubishi IGBT module [37]. The life time of the module in thermal cycling has been enhanced by optimizing IMB insulating material and thickness, and a 23% increment of the effective chip-contacting area has been achieved.

2) Advanced Die-Attaching Materials

Soft solder is the most commonly used packaging material in power electronics. But its low thermal conductivity and melting point limits the power devices to operate up to 175 °C, which cannot fully exploit high temperature advantage of the WBG devices. Moreover, the lead solder is harmful to human's health and the environment, so the lead-free die-attaching materials are preferred. The nano silver sintering and transient liquid phase bonding (TLPB) are two promising alternatives.

a) Nano Silver Sintering

Nano silver sintering is a low temperature joining technique (LTJT). Due to the size effect, the melting point of silver particles in nano and micro scale is far below that of silver bulk [10], [23]-[26]. By applying a certain pressure and temperature of above 220 °C, silver particles will be melted and sintered spontaneously under the effect of liquid phase capillary force. The sintered silver has high thermal conductivity (250 W/mK), high electrical conductivity (41 MS/m) and high melting point (close to 961 °C). It has demonstrated good mechanical characteristics with a CTE value of 19 μm/mK and a tensile strength of 55 MPa. So far, silver sintering has been applied to industrial manufacturing for a range of selected products. But it is not a versatile approach for mass manufacturing mainly due to the quality issues and failures in silver-sintered contact interfaces. This sintering technique needs to be further improved.

b) Transient Liquid Phase Bonding

TLPB uses the diffusion between a high melting point and a low melting point material [19]. Many materials such as Ag/In, Ag/Sn, Au/In, Au/Sn, Cu/Sn, and Ni/Sn can be used as the soft solder with lower melting point. In the process of TLPB, the first step is to melt the low melting point material to form intermetallic phase (IMP) between the liquid and solid phase. Then after all the liquid phase transformed to IMP, a recommended maximum pressure of 0.3 MPa is required to contact the substrates while avoiding squeezing out of the liquid phase. The solid bond shows a higher remelting temperature than the initial process temperature. It has been reported that the IMC ε-phase Ag_3Sn has a melting temperature of 480 °C and the ζ-phase Ag_5Sn with a melting temperature of up to 724 °C, which are much higher than that of pure Sn with 232 °C.

3) Encapsulation Materials

Encapsulation provides protection for power module against mechanical stress, electrical breakdown, chemical erosions, α radiations, and so on. However, conventional encapsulations are only suitable for applications below 175 °C. To achieve higher operating temperature, the new encapsulation materials should have the characteristics, e.g. high thermal conductivity, close CTE to semiconductor materials, high dielectric strength, etc. Several encapsulants are reported to be able to operate above 250 °C. However, some of their properties may degrade when the temperature is close to 250 °C [52], [53]. As for underfills and molding compounds, their low glass-transition temperature (T_g) limits the high temperature operation, so appropriate modification of the chemical composition is required to achieve higher T_g. High-T_g polymers, such as polyimide, bismaleimide, and cyanate ester, are potential encapsulants for high-temperature (>250 °C) operation. However, the internal stress caused by mismatching CTE with semiconductors needs to be limited. Potting compounds limited by their thermal decomposition also need appropriate modification to improve thermal stability [11].

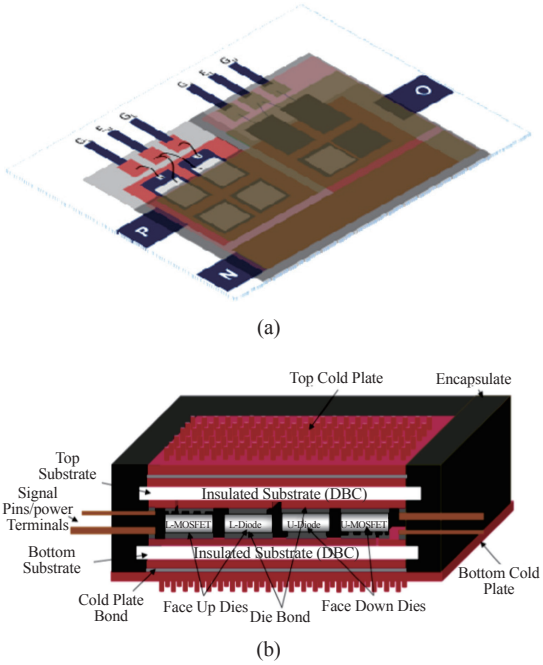


Fig. 7. Integrated double-sided cooling packaging structure [29]. (a) Aerial view of a planar-bond-all phase leg power module. (b) Cross sectional view of the module with dual cold plates.

C. Advanced Packaging Structures

In traditional power modules, a 2D layout structure is employed, in which the heat is transferred in one direction and the parasitic inductance of the interconnections are large. The more advanced structures, including 2.5D structures and 3D structures which can achieve double-sided cooling and smaller parasitic inductance, are preferred for high power density applications.

In the 2.5D structures, there are usually two substrates, one of which is for the attachment of power chips and heat sink, and the other is for interconnection [30]. In addition, copper pin, metal post or shim material is required to match the height difference between MOSFET/IGBT and diode dies [37]. The most representative packaging technology is the planar-bond-all technology which features three-dimensional planar electrical interconnection and double-sided cooling [29], [31], [32], shown in Fig. 7. The advanced packaging structure can achieve 75% reduction in parasitic inductance and 40% reduction in thermal resistance. Another typical 2.5D packaging structure is Semikron's all-sintered SKiN® package [27], [28], shown in Fig. 8. All solder and bond wire contacts are eliminated by using silver diffusion sintering joints, and the flex foil is firstly introduced for interconnections. In this structure, the parasitic inductance can be reduced up to 10%.

The 3D packaging structure is a novel concept based on stacking power dies [30], which can achieve ultra-low parasitics, compact package and excellent thermal performance. The chip-on-chip (CoC) structure proposed by Nottingham is a representative 3D structure [33], in which two power chips are vertically stacked and connected through vias,

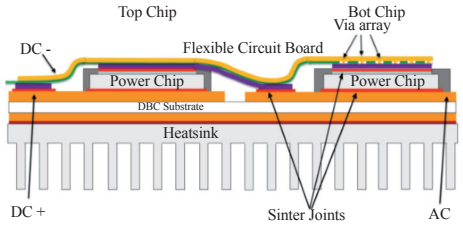


Fig. 8. SKiN® packaging structure [27].

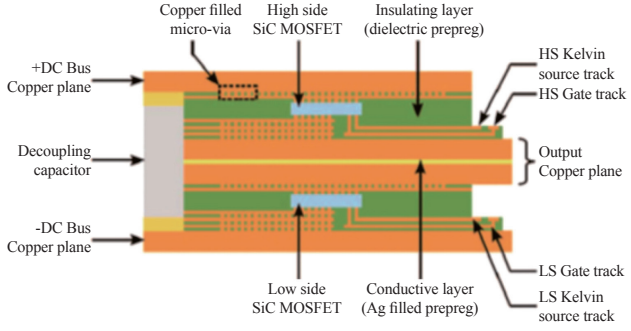


Fig. 9. CoC 3D power module structure [34].

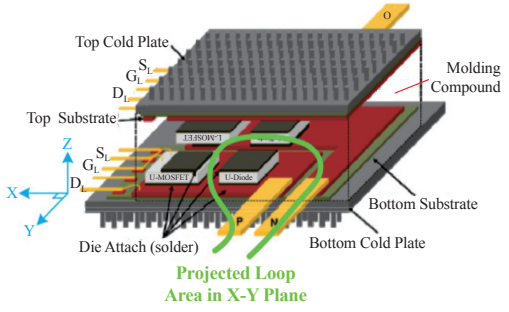


Fig. 10. Baseline power module.

copper or solder bumps etc. The 3D structure shown in Fig. 9 was proposed in [34], which demonstrates an ultra-low inductance of only 0.25 nH.

D. Module-Level Integration

Integrating the power chips with some associate components into a module can bring many benefits, such as reduced parasitics, improved thermal conductivity. The associate components which can be integrated into the module include the decoupling capacitors, gate drivers, temperature sensors, current sensors, protection circuits, etc.

The integration of decoupling capacitor is to reduce the power loop inductance by eliminating the parasitic inductance between the connection of module to external circuit. The module integrated with the decoupling capacitor shown in Fig. 11, achieves over 60% reduction of power loop parasitic inductance (just 1.63 nH) compared with the baseline module [36] in Fig. 10. The method of integrating decoupling capacitor to reduce power loop inductance was also demonstrated in [54]. Furthermore, the integration of double sided fin-pin heatsinks in Fig. 10 and Fig. 11 shows improved heat-dissipation capability.

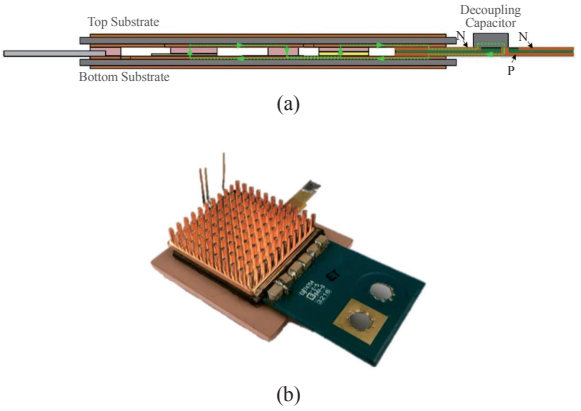


Fig. 11. Double sided cooling power module with integrated decoupling capacitor. (a) Current commutation loop illustration. (b) Fabricated power module [36].

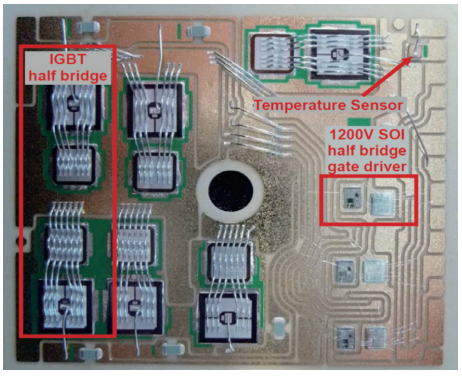


Fig. 12. A 1200 V/50 A module with integrated gate drive and temperature sensor [55].

The integration of gate driver can realize low gate loop inductance, which can reduce the gate overvoltage and ringing. [55] demonstrates a 1200 V/50 A IPM with integrated gate driver and a temperature sensor, as shown in Fig. 12. In [56], the gate driver was also integrated into a SiC half-bridge module based on the silicon-on-insulator technology. Because of the ultra-low gate loop inductance by integrating gate driver, the gate resistor can be eliminated. The integration of temperature sensor in Fig. 12 can provide the temperature information for monitoring and studying the module aging. Except the temperature sensor, current sensor can also be integrated into module. A monolithic current sensor is integrated in a SiC MOSFET module [57].

III. Passive Integration Technologies

Passive devices, especially magnetic components, often occupy a considerable volume, and become one of the main bottlenecks to improve the power density of the converters. Integrating multiple passive components can reduce their number, size and cost. This section will review some passive integration technologies, including magnetic integration technology, electromagnetic integration technology, Pwr-

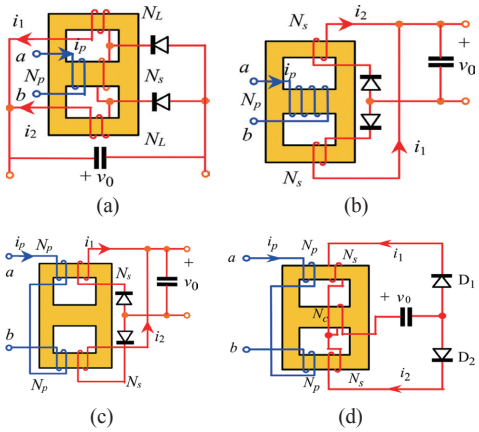


Fig. 13. Magnetic structure of CDR [61].

SOC and PwrSiP technology, and LTCC integration technology.

A. Magnetic Integration Technology

The magnetic components, namely inductors and transformers, occupy a considerable space of the total volume, which have harmful effects to the power density. To solve this problem, the magnetics are integrated into one core. There are many converters have applied the magnetic integration technology. For example, Cuk converter and forward converter are integrated into a single core by Slobodan. Cuk [38] and G. D. Bloom [39], [58], [59], respectively. An improvement of forward converter is made in [60]. The three magnetic components of the current-doubler rectifier (CDR) are integrated into single integrated component [61], shown in Fig. 13(a). To minimize the termination loss, the windings are integrated [62], shown in Fig. 13(b). An improvement is made by [63] [64]. The windings at the center leg are spilt into the two outer legs, resulting in increasing in coupling coefficient of primary and secondary, shown in Fig. 13(c). The filtering inductance in aforementioned topology has a limited value. A new design with increasing filter inductance is proposed in [65], shown in Fig. 13(d). But the increasing of the secondary windings that conduct large current, induces large winding losses. Thus, a trade-off between filter inductance and winding losses should be made. Some topologies have already implemented the integrated CDR to increase power density and reduce power losses [66], [67].

Another typical application of magnetic integration is for multiphase converter of which the inductors are integrated into one magnetics. The integrated inductors [68] can be divided into noncoupled inductors [69] and coupled inductors [70]. The integrated inverse coupled inductors can not only reduce current ripple by increasing steady state inductance, but also increase transient respond by decreasing transient inductance [41], [71]. As the interleaved phases increase, the asymmetry of the circuit as well as the complexity in design and control increase with limited benefits [72]. Although inverse coupled inductors have better performance in steady state and transient state than noncoupled inductors, winding path of coupled inductors is much larger. A twisted core coupled inductor is proposed [73], shown in Fig. 14. In [74], a lateral coupled inductor using ferrite material is proposed, shown in Fig. 15.

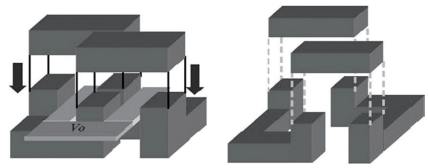


Fig. 14. Structure of the twisted core coupled inductor [73].

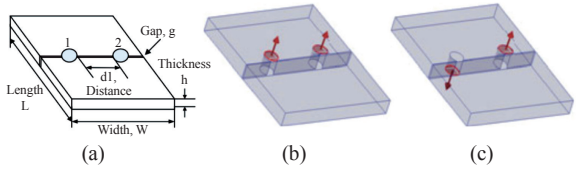


Fig. 15. Two-phase lateral-coupled inductor structure [74]. (a) Dimensions. (b) Direct coupling. (c) Inverse coupling.

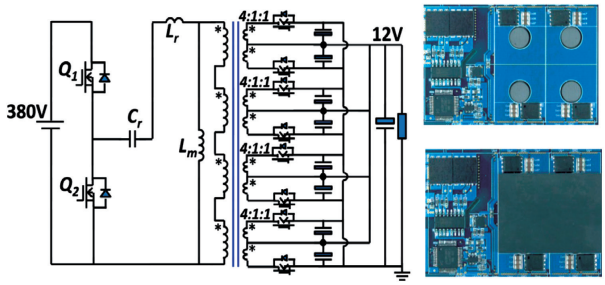


Fig. 16. Structure of integrated matrix transformer [77].

In addition, the magnetic integration is also employed in some resonant converters, such as LLC converter [42], [43]. The resonant inductor of LLC converter is realized by large leakage inductance of transformer. In order to achieving large inductance, an auxiliary core around primary windings and a low permeability layer between the primary and secondary are proposed in [43] and [42], respectively. For high output current situation, LLC converter with matrix transformer is proposed [75], [76]. The transformer consists of two cores, each of which integrates two matrix components. To further improve power density, a novel structure integrated four matrix transformer of LLC converter is proposed by CPES [77], achieving power density of 900 W/in^3, shown in Fig. 16. Shielding technique is used to reduce EMI effect of LLC converter with matrix transformer at high frequency [78].

B. Electromagnetic Integration Technology

To further reduce the number and size of the passive components, the electromagnetic integration that combines the magnetics and capacitors is developed. The integrated passive module can be used in resonant applications [79], non-resonant [80] applications, as well as used as EMI filters [81]-[83].

An integrated LC structure is proposed [84]-[86], shown in Fig. 17(a). The structure has a dielectric material sandwiched between two planar conductors, and a module having distrib-

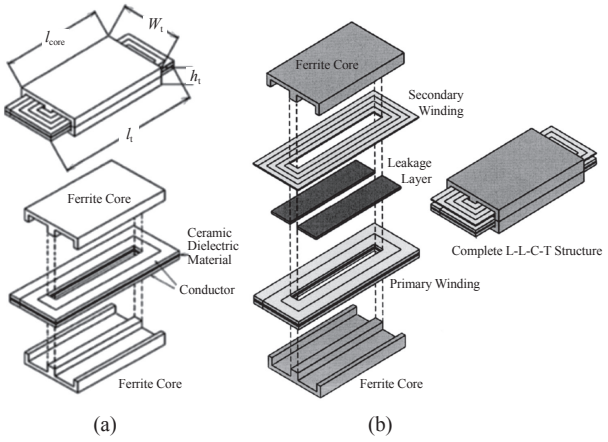


Fig. 17. Structure of LC and LLCT module [91].

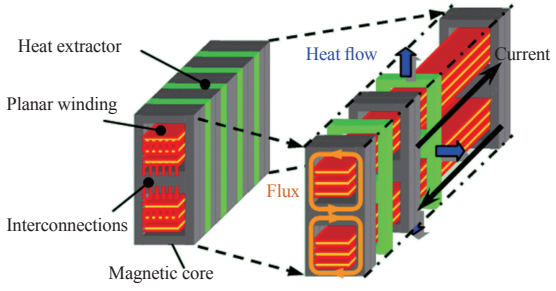


Fig. 18. Structure of heat extractor [99].

uted inductance and capacitance is formed. To further save space, capacitors, inductors and transformers are integrated together, forming the integrated LCT module [87]-[90]. For the resonant tank that contains magnetizing inductance, the structure of LLCT is obtained, shown in Fig. 17(b).

However, the optimized volume can't be achieved without accurate electromagnetic design and loss model. For the sake of the optimized design of the integrated module, electromagnetic model and design as well as loss calculation are developed [91]-[97]. Besides, to ensure the reliable operation, thermo-mechanical analysis is described in [98]. To further improve the power density without exceeding the highest temperature of material, a method for heat dissipation is essential. In [99], heat extractors are embedded into the magnetic core, shown in Fig. 18. A prototype that can achieve power density more than 1 kW/in^3 is obtained.

The LLCT modules have been implemented into resonant converter such as LLC resonant converter and non-resonant converter, namely asymmetrical half-bridge pulse width-modulation converter (AHBC) [44], [80], [100]. In [44], the LLC resonant tank is integrated into LLCT module, as shown in Fig. 19(a). The volume of passive integrated module is reduced to 14.6 cm^3. In [80], LLCT modules are implemented into current-doubler rectifier. To save the footprint, two LLCT modules are integrated into a single planar magnetic core, shown in Fig. 19(b). The total volume is 60 cm^3, which is much smaller than the discrete module. Therefore, by using LLCT module in the converter, the profile and volume can be decreased.

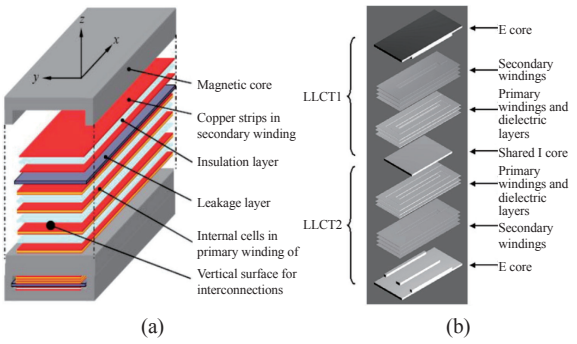


Fig. 19. (a) LLCL module structure of LLC converter [44]. (b) Current-doubler rectifier [80].

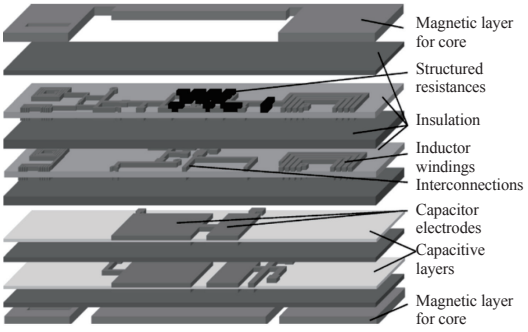


Fig. 20. Principle of emPIC proposed in [102].

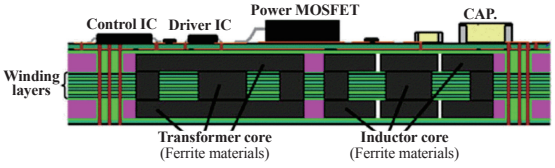


Fig. 21. Structure of emPIC proposed in [104].

To fully utilize the space and increase the heat dissipation ability, embedded passives integrated circuit (emPIC) is proposed [101]-[104]. In [102], capacitive layers and magnetic components are embedded in the PCB, shown in Fig. 20. The magnetic layers are achieved by utilizing ferrite polymer compounds named MagLam. In [104], a transformer and a inductor, using ferrite material having high permeability and low loss property, are integrated into PCB, shown in Fig. 21. An-eighth-brick with power density of 553 W/in^3 is obtained.

C. Power Supply on Chip and Power Supply in Package

A higher-level integration is to integrate the magnetic components with other components of the converter together, including the switches, drivers, and controllers. This kind of integration is possible to obtain a very high-power density, along with improved reliability and efficiency. At present, the technology is mainly used for low voltage and low power applications due to its complexity. The integration technology can be classified into two categories as PwrSiP and PwrSoC [105]-[107].

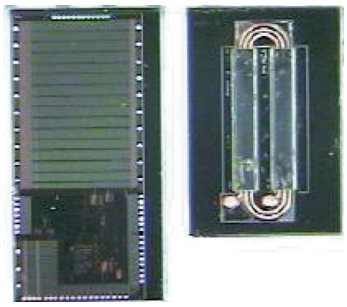


Fig. 22. A 20 MHz DC-DC converter IC and a 100 nH micro-inductor [108].

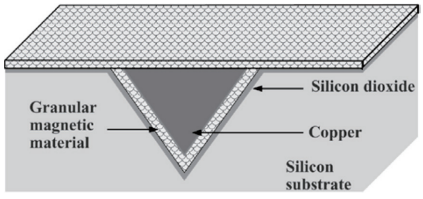
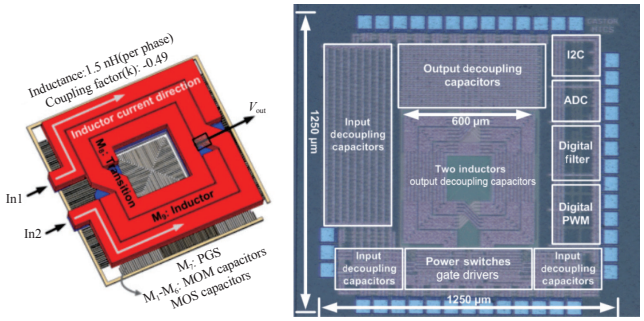


Fig. 23. Schematic of a V-groove inductor [110].



(a) (b)

Fig. 24. (a) Structure of a coupled air-core inductor. (b) Layout of the 500 MHz prototype IC [112].

PwrSoC is a wafer-level integration where the magnetic components are built in or on silicon die. A typical example is micro-inductor built on silicon for a 20 MHz DC-DC converter in Fig. 22 [108]. The coil is typically formed by depositing conductor on silicon wafers with a maximum thickness of 50 μm. The thickness of the magnetic material covering the coil is generally limited to within 10 μm. This inductor can only handle 500 mA of currents due to the limited coil thickness. R. Meere *et al*. builds a 100 MHz magnetic core inductor on silicon wafer, and it shows higher efficiency than a comparable air core inductor on silicon even at 100 MHz [109]. P. Dhagat *et al*. proposes a V-groove inductor to increase the current capability [110]. A V-shaped groove is formed on the silicon substrate by etching, as shown in Fig. 23. More copper materials can be deposited in the groove to form a thicker coil conductor, and as a result, this inductor can handle up to 7 A of current. More researches have conducted to further optimize this V-groove inductor [111]. Another typical example is the air-core inductor presented in [112]. The converter's operating frequency is pushed to 500 MHz, where the inductor needs only a very small value of 1.54 nH. This inductor was fabricated in a

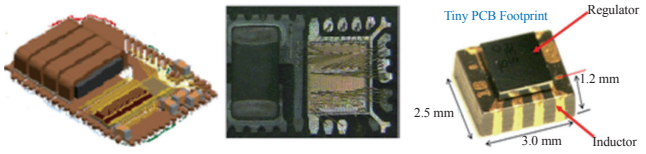


Fig. 25. Commercial PwrSiP products [107].

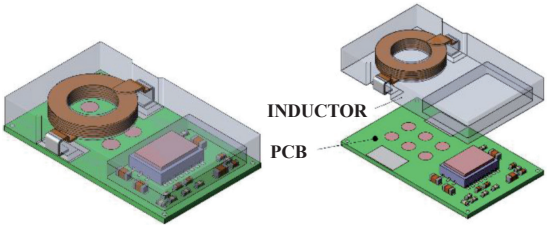
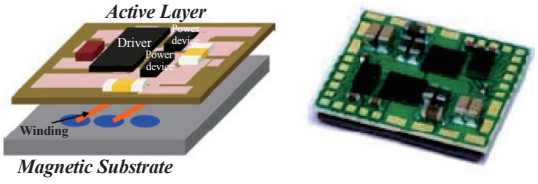


Fig. 26. Schematic of a power-system-in-inductor module [113].



(a) (b)

Fig. 27. 3D integration POL converter [115]. (a) Schematic. (b) Prototype of a two-phase interleaved converter.

65 nm CMOS chip. The output capacitor is also integrated into the chip. The total area occupied by the inductor and capacitor is only 1.1 mm^2, as shown in Fig. 24.

PwrSiP is to package a full converter into a single module, in which the magnetics and other components are connected internally. Compared to PwrSoC, PwrSiP is easier to be built and it can handle more power. Many companies have launched their own products [107], as shown in Fig. 25. To further improve the power density, many studies have been carried out. A power-system-in-inductor structure is proposed in [113], [114] where magnetic component is used as a package housing and the whole converter is packaged within the magnetic component, as shown in Fig. 26. Compared with the traditional plastic packaging structure, the inductor can gain much more space in the same package. As a result, the inductor can obtain greater inductance value and smaller DC resistance, which helps to improve the converter's efficiency. In addition, the thermal performance of the module can be improved because the thermal conductivity of the magnetic material is higher than that of the plastic material. Another typical example is the 3D integrated point of load (POL) converter proposed by CPES [115], [116]. Fig. 27 shows the concept of a 3D integrated POL converter. The active devices are soldered on the one side of the PCB or DBC substrate, and a low profile LTCC inductor is placed on the other side of the substrate. This module can operate at up to 5 MHz [117]. The power density of the 3D integrated POL converter can achieve a power density of as high as 1100 W/in^3, which is around 10 times higher than that of industry products at the same current level.

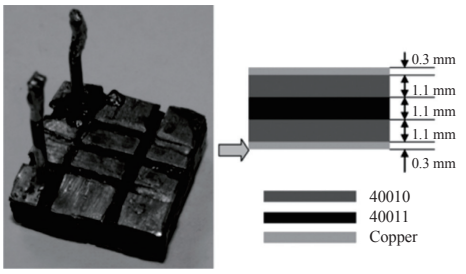


Fig. 28. Prototype of the nonlinear LTCC inductor [125].

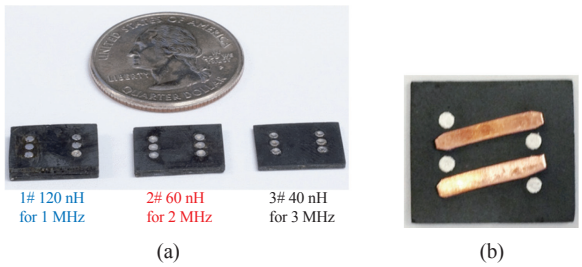


Fig. 29. LTCC inductors [129]. (a) LTCC cores at different frequencies. (b) Two phases coupled LTCC inductor.

D. LTCC Integration Technology

The LTCC material is made of ferrite tapes and ceramic tapes through stacking, pressing, co-firing and other steps [118]. It can be used to build passive components with low profile and flexible structure, which can help improve space utilization and facilitate integration [115], [119]. The CTE of LTCC material is around 5 ppm/°C, which is close that of silicon material, so that hybrid integration could be easily realized. The LTCC material also has higher thermal conductivity than FR4 used in PCB and thus features better thermal management.

An ultrathin coupled inductor based on LTCC technology was fabricated in [120], [121] for an interleaved buck converter. The thickness of the LTCC coupled inductor is only 1.3 mm. Another advantage of the LTCC inductor is that it has a distributed air gap, which is beneficial to reduce the AC loss of the winding when compared with the traditional air gap inductor. However, the flux density distribution of the distributed air-gap LTCC inductor is not uniform in the magnetic cores, which can cause the magnetic core near the conductor to saturate easily while the core away from the conductor is not fully utilized. To address this problem, Wang *et al*. [122]-[124] proposes a multi-permeability distributed air-gap magnetic structure. The internal permeability is lower than the external permeability, so a more uniform magnetic flux density distribution can be obtained. The multi-permeability LTCC inductor can achieve higher inductance value and relatively stable inductance value than the single permeability LTCC inductor without increasing the inductor size. A nonlinear LTCC inductor is proposed in [125]-[127]. The core of the LTCC inductor is made of ferrite tapes with different permeability. As the DC current increases, the ferrite tapes with high permeability gradually saturates, causing the inductance to drop gradually. This nonlinear inductor has a relatively large light-load inductance, which can help reduce light-load current ripple and thus improve the light-load efficiency. Fig. 28 shows a prototype of the nonlinear LTCC inductor with two different permeability.

CPES has conducted a series of studies for 3D POL integration using the low profile LTCC inductors as a substrate [128]-[136]. The use of low profile inductors allows for more efficient use of space when integrated with the active devices. Fig. 29 shows the LTCC inductors substrate. As the frequency increases, the LTCC inductor can be made thinner, thereby increasing the power density. To obtain a better performance of the LTCC inductor substrate, some studies have been carried out. The characteristtics of the LTCC ferrite tape is explored detailly in [137]. Li *et al*. [136] proposed several models to calculate inductance for the LTCC inductor. A numerical model is proposed in [138] and an analytical model is proposed in [139] to calculate the core loss. Based on these studies, the LTCC inductor substrate is fully optimized for 3D integrated POL converter. Along with the layout optimization to reduce parasitic inductance, the use of DBC substrate to enhance heat dissipation, and the use of GaN devices to reduce switching losses, the switching frequency of the 3D integrated POL converter is pushed up to 5MHz [117]. Furthermore, a two phase LTCC coupled inductor is designed for the 3-D integrated POL converter, in which the frequency of the AC magnetic flux of the LTCC inductor reaches 10 MHz. The core thickness of the LTCC coupled inductor is only 0.4 mm.

IV. Conclusions

This paper reviews the state-of-the-art integration technologies involving active and passive integrations. The active integration technologies are reviewed from the aspects of interconnection technology, packaging material technology, packaging structure technology, and module-level integration technology. The emergence of wide band-gap semiconductor devices puts forward higher requirements for active integration technologies, especially parasitic and cooling issues. Great advancements have been made in active integration technologies. 1) Advanced wirebond-less technologies and advanced packaging structures (including 2.5D structures and 3D structures) have been developed to realize small parasitics and high heat-dissipation capability; 2) Emerging die-attaching materials, such as nano-silver sintering and TLPB, have demonstrated excellent high-temperature performance, and are promising for high power density applications; 3) The modules with integrated gate driver, decoupling capacitor, sensors, and heat sinks, etc. have been developed to achieve better performance. The passive integration technologies are reviewed from the aspects of the magnetic integration technology, electromagnetic integration technology, PwrSoC and PwrSiP technology, and LTCC integration technology. Magnetic integration technology and electromagnetic integration technology can effectively reduce the size of passive components, and have been applied to the various circuits, such as current-doubler rectifier, multiphase

converter, LLC converter, etc. PwrSoC is a wafer-level integration and suitable for low current (below several amps) applications, while PwrSiP can handle currents up to 40 A. CPES has successfully developed a 3D integrated module with power density up to 1100 W/in^3. The LTCC magnetics have been successfully applied to high-frequency high-current 3D integrated module, and are expected to be extended to higher power integrated modules.

References

[1] Z. Liang, F. Wang, and L. Tolbert, "Development of packaging technologies for advanced SiC power modules," in *Wide Bandgap Power Devices and Applications,* 2014, pp. 42-47.

[2] Y. Xie, Y. Li, Z. Huang, T. Liu, Y. Zhang, Y. Tan, *et al*., "Using ultra-low parasitic hybrid packaging method to reduce high frequency EMI noise for SiC power module," in *2017 IEEE 5th Workshop on Wide Bandgap Power Devices and Applications (WiPDA)*, 2017, pp. 201-207.

[3] L. Ménager, M. Soueidan, B. Allard, V. Bley, and B. Schlegel, "A lab-scale alternative interconnection solution of semiconductor dice compatible with power modules 3-D integration," *IEEE Transactions on Power Electronics,* vol. 25, no. 7, pp. 1667-1670, 2011.

[4] Z. Liang, P. Ning, F. Wang, and L. Marlino, "A phase-leg power module packaged with optimized planar interconnections and integrated double-sided cooling," *IEEE Journal of Emerging & Selected Topics in Power Electronics,* vol. 2, no. 3, pp. 443-450, 2014.

[5] Y. Pascal, A. Abdedaim, D. Labrousse, M. Petit, S. Lefebvre, and F. Costa, "Using laminated metal foam as the top-side contact of a PCB-embedded power die," *IEEE Electron Device Letters,* vol. PP, no. 99, pp. 1-1, 2017.

[6] D. Domes, C. Messelke, and P. Kanschat, "1st industrialized 1200 V SiC JFET module for high energy efficiency applications."

[7] T. Nakamura, M. Aketa, Y. Nakano, M. Sasagawa, and T. Otsuka, "Novel developments towards increased SiC power device and module efficiency," in *Energytech*, 2012, pp. 1-6.

[8] S. Nakata, N. Miura, and Y. Nakaki, "SiC power device technology," 2011.

[9] C. Durand, M. Klingler, D. Coutellier, and H. Naceur, "Power cycling reliability of power module: A survey," *IEEE Transactions on Device & Materials Reliability,* vol. 16, no. 1, pp. 80-97, 2016.

[10] C. Göbl and J. Faltenbacher, "Low temperature sinter technology die attachment for power electronic applications," in *International Conference on Integrated Power Electronics Systems,* 2011, pp. 1-5.

[11] Y. Yao, G. Q. Lu, D. Boroyevich, and K. D. T. Ngo, "Survey of high-temperature polymeric encapsulants for power electronics packaging," *IEEE Transactions on Components Packaging & Manufacturing Technology*, vol. 5, no. 2, pp. 168-181, 2017.

[12] Y. Zhao, P. Mumby-Croft, S. Jones, A. Dai, Z. Dou, Y. Wang *et al*., "Silver sintering die attach process for IGBT power module production," in *Applied Power Electronics Conference and Exposition,* 2017, pp. 3091-3094.

[13] J. Yin, J. D. Van Wyk, W. G. Odendaal, and Z. Liang, "Design and optimization of embedded power chip modules for double-sided cooling," in *Industry Applications Conference, 2004. Ias Meeting. Conference Record of the*, 2004, pp. 1545-1551 vol.3.

[14] S. S. Wen, D. Huff, and G. Q. Lu, "Dimple-array interconnect technique for packaging power semiconductor devices and modules," in *International Symposium on Power Semiconductor Devices and ICS*, 2001, pp. 69-74.

[15] B. C. Charboneau, F. Wang, J. D. V. Wyk, D. Boroyevich, Z. Liang, E. P. Scott *et al*., "Double-sided liquid cooling for power semiconductor devices using embedded power packaging," *IEEE Transactions on Industry Applications,* vol. 44, no. 5, pp. 1645-1655, 2008.

[16] Z. Liang and F. C. Lee, "Embedded power technology for IPEMs packaging applications," in *Applied Power Electronics Conference and Exposition, 2001. Apec 2001. Sixteenth IEEE*, 2001, pp. 1057-1061, vol.2.

[17] Z. Liang, J. D. V. Wyk, and F. C. Lee, "Embedded power: a 3-D MCM integration technology for IPEM packaging application," *IEEE Transactions on Advanced Packaging*, vol. 29, no. 3, pp. 504-512, 2006.

[18] S. S. Wen, D. Huff, and G. Q. Lu, "Enhancement of thermal fatigue reliability of power semiconductor interconnects using dimple-array solder joints," in *Power Electronics Specialists Conference, 2001. Pesc. 2001 IEEE,* 2001, pp. 1926-1931 vol. 4.

[19] J. G. Bai, G. Q. Lu, and X. Liu, "Flip-chip on flex integrated power electronics modules for high-density power integration," *Advanced Packaging IEEE Transactions on,* vol. 26, no. 1, pp. 54-59, 2003.

[20] F. C. Lee, J. D. Van Wyk, D. Boroyevich, and G. Q. Lu, "Technology trends toward a system-in-a-module in power electronics," *Circuits & Systems Magazine IEEE*, vol. 2, no. 4, pp. 4-22, 2002.

[21] J. N. Calata, J. G. Bai, X. Liu, S. Wen, and G. Q. Lu, "Three-dimensional packaging for power semiconductor devices and modules," *IEEE Transactions on Advanced Packaging*, vol. 28, no. 3, pp. 404-412, 2005.

[22] P. Natzke, U. Grossner, J. Janczak-Rusch, and L. Jeurgens, "Thin layer Ag-Sn transient liquid phase bonding using magnetron sputtering for chip to baseplate bonding," in *2017 IEEE 5th Workshop on Wide Bandgap Power Devices and Applications (WiPDA)*, 2017, pp. 165-170.

[23] J. G. Bai, J. Yin, Z. Zhang, G. Q. Lu, and J. D. V. Wyk, "High-temperature operation of SiC power devices by low-temperature sintered silver die-attachment," *IEEE Transactions on Advanced Packaging,* vol. 30, no. 3, pp. 506-510, 2007.

[24] G. Q. Lu, J. N. Calata, G. Lei, and X. Chen, "Low-temperature and pressureless sintering technology for high-performance and high-temperature interconnection of semiconductor devices," in *International Conference on Thermal, Mechanical and Multi-Physics Simulation Experiments in Microelectronics and Micro-Systems, 2007. Eurosime,* 2007, pp. 1-5.

[25] J. G. Bai, Z. Z. Zhang, J. N. Calata, and G. Q. Lu, "Low-temperature sintered nanoscale silver as a novel semiconductor device-metallized substrate interconnect material," *IEEE Transactions on Components & Packaging Technologies,* vol. 29, no. 3, pp. 589-593, 2006.

[26] J. G. Bai, J. N. Calata, and G. Q. Lu, "Processing and characterization of nanosilver pastes for die-attaching SiC devices," *IEEE Transactions on Electronics Packaging Manufacturing,* vol. 30, no. 4, pp. 241-245, 2007.

[27] P. Beckedahl, S. Buetow, A. Maul, M. Roeblitz, and M. Spang, "400 A, 1200 V SiC power module with 1nH commutation inductance," in *Cips 2016; International Conference on Integrated Power Electronics Systems; Proceedings of,* 2016.

[28] P. Beckedahl, M. Spang, and O. Tamm, "Breakthrough into the third dimension—Sintered multi layer flex for ultra low inductance power modules," in *International Conference on Integrated Power Systems*, 2014, pp. 1-5.

[29] Z. Liang, "Integrated double sided cooling packaging of planar SiC power modules," in *Energy Conversion Congress and Exposition,* 2015, pp. 4907-4912.

[30] J. Schuderer, U. Vemulapati, and F. Traub, "Packaging SiC power semiconductors—Challenges, technologies and strategies," in *Wide Bandgap Power Devices and Applications,* 2014, pp. 18-23.

[31] Z. Liang, P. Ning, F. Wang, and L. Marlino, "Planar bond all: A new packaging technology for advanced automotive power modules," in *Energy Conversion Congress and Exposition*, 2012, pp. 438-443.

[32] Z. Liang, "Planar-bond-all: A technology for three-dimensional integration of multiple packaging functions into advanced power modules," in *IEEE International Workshop on Integrated Power Packaging,* 2015, pp. 115-118.

[33] J. F. Li, A. Castellazzi, A. Solomon, and C. M. Johnson, "Reliable integration of double-sided cooled stacked power switches based on 70 micrometer thin IGBTs and diodes," in *International Conference on Integrated Power Electronics Systems,* 2012, pp. 1-6.

[34] G. Regnat, P. O. Jeannin, G. Lefevre, J. Ewanchuk, D. Frey, S. Mollov *et al*., "Silicon carbide power chip on chip module based on embedded die technology with paralleled dies," in *Energy Conversion Congress and Exposition,* 2015, pp. 4913-4919.

[35] C. Qiaoliang, P. Yunqing, Y. Xu, and W. Zhaoan, "Analysis and suppression of inductive interference in an active integrated power elec-

tronics module," *IEEE Transactions on Components and Packaging Technologies,* vol. 32, no. 4, pp. 724-733, 2009.

[36] F. Yang, Z. Liang, Z. J. Wang, and F. Wang, "Design of a low parasitic inductance SiC power module with double-sided cooling," in A*pplied Power Electronics Conference and Exposition,* 2017, pp. 3057-3062.

[37] C. Chen, "A review of SiC power module packaging: Layout, material system and integration," 2017.

[38] S. Ćuk, "A new zero-ripple switching dc-to-dc converter and integrated magnetics," in *1980 IEEE Power Electronics Specialists Conference,* 1980, pp. 12-32.

[39] G. E. Bloom and R. Severns, "The generalized use of integrated magnetics and zero-ripple techniques in switchmode power converters," in *Power Electronics Specialists Conference, 1984 IEEE*, 1984, pp. 15-33.

[40] H. Zhou, T. X. Wu, I. Batarseh, and K. D. T. Ngo, "Comparative investigation on different topologies of integrated magnetic structures for current-doubler rectifier," in *2007 IEEE Power Electronics Specialists Conference,* 2007, pp. 337-342.

[41] W. Pit-Leong, X. Peng, P. Yang, and F. C. Lee, "Performance improvements of interleaving VRMs with coupling inductors," *IEEE Transactions on Power Electronics,* vol. 16, no. 4, pp. 499-507, 2001.

[42] M. Meinhardt, M. Duffy, T. O. Donnell, S. O. Reilly, J. Flannery, and C. O. Mathuna, "New method for integration of resonant inductor and transformer-design, realisation, measurements," in *Applied Power Electronics Conference and Exposition, 1999. APEC '99. Fourteenth Annual,* 1999, pp. 1168-1174 vol.2.

[43] A. Kats, G. Ivensky, and S. Ben-Yaakov, "Application of integrated magnetics in resonant converters," in *Proceedings of APEC 97–Applied Power Electronics Conference,* 1997, pp. 925-930 vol.2.

[44] D. Huang, D. Gilham, W. Feng, P. Kong, D. Fu, and F. C. Lee, "High power density high efficiency dc/dc converter," in *2011 IEEE Energy Conversion Congress and Exposition,* 2011, pp. 1392-1399.

[45] B. Passmore, Z. Cole, B. Mcpherson, B. Whitaker, D. Martin, A. Barkley *et al., Wide bandgap packaging for next generation power conversion systems*, 2013.

[46] Z. Chen, Y. Yao, D. Boroyevich, K. D. T. Ngo, P. Mattavelli, and K. Rajashekara, "A 1200-V, 60-A SiC MOSFET multichip phase-leg module for high-temperature, high-frequency applications," *IEEE Trans. Power Electron.,* vol. 29, no. 5, pp. 2307-2320, 2014.

[47] M. Wang, F. Luo, and L. Xu, "A double-end sourced multi-chip improved wire-bonded SiC MOSFET power module design," in *Applied Power Electronics Conference and Exposition,* 2016, pp. 709-714.

[48] R. Wang, D. Boroyevich, P. Ning, Z. Wang, F. Wang, P. Mattavelli *et al*., "A high-temperature SiC three-phase AC–DC converter design for > 100/spl deg/C ambient temperature," *IEEE Transactions on Power Electronics,* vol. 28, no. 1, pp. 555-572, 2012.

[49] Z. Chen, Y. Yao, D. Boroyevich, and K. Ngo, "An ultra-fast SiC phase-leg module in modified hybrid packaging structure," in *Energy Conversion Congress and Exposition,* 2014, pp. 2880-2886.

[50] C. Chen, Y. Chen, Y. Li, Z. Huang, T. Liu, and Y. Kang, "A SiC-based half-bridge module with improved hybrid packaging method for high power density applications," *IEEE Transactions on Industrial Electronics,* vol. PP, no. 99, pp. 1-1, 2017.

[51] R. Khazaka, L. Mendizabal, D. Henry, and R. Hanna, "Survey of high-temperature reliability of power electronics packaging components," *IEEE Trans. Power Electron.,* vol. 30, no. 5, pp. 2456-2464, May 2015.

[52] Y. Y. Yao, Z. Chen, G. Q. Lu, D. Boroyevich, and K. D. T. Ngo, "Characterization of encapsulants for high-voltage high-temperature power electronic packaging," *Ieee T Comp Pack Man*, vol. 2, no. 4, pp. 539-547, Apr. 2012.

[53] J. D. Scofield, J. N. Merrett, J. Richmond, A. Agarwal, and S. Leslie, "Performance and reliability characteristics of 1200 V, 100 A, 200 °C half-bridge SiC MOSFET-JBS diode power modules," vol. 2010, no. HITEC, 2010.

[54] Y. Ren, X. Yang, F. Zhang, L. L. Wang, K. P. Wang, W. J. Chen *et al*., "Voltage suppression in wire-bond-based multichip phase-leg SiC MOSFET module using adjacent decoupling concept," *IEEE Trans. Ind. Appl.,* vol. 64, no. 10, pp. 8235-8246, Oct. 2017.

[55] B. Vogler, M. Rossberg, R. Herzer, and L. Reusser, "Integration of 1200 V SOI gate driver ICs into a medium power IGBT module package," in *International Symposium on Power Semiconductor Devices & Ic's,* 2009, pp. 97-100.

[56] H. A. Mantooth, M. D. Glover, and P. Shepherd, "Wide bandgap technologies and their implications on miniaturizing power electronic systems," *IEEE Journal of Emerging and Selected Topics in Power Electronics,* vol. 2, no. 3, pp. 374-385, Sept. 2014.

[57] M. Berthou, P. Godignon, and J. Millan, "Monolithically integrated temperature sensor in silicon carbide power MOSFETs," *IEEE Transactions on Power Electronics,* vol. 29, no. 9, pp. 4970-4977, Sept. 2014.

[58] E. Bloom, "Core selection for & design aspects of an integrated-magnetic forward converter," in *1986 IEEE Applied Power Electronics Conference and Exposition,* 1986, pp. 141-150.

[59] E. Bloom, "New integrated-magnetic DC-DC power converter circuits & systems," in *Applied Power Electronics Conference and Exposition, 1987 IEEE*, 1987, pp. 57-66.

[60] Q. Chen, Y. Feng, L. Zhou, J. Wang, and X. Ruan, "An improved active clamp forward converter with integrated magnetics," in *2007 IEEE Power Electronics Specialists Conference,* 2007, pp. 377-382.

[61] S. Jian, K. F. Webb, and V. Mehrotra, "An improved current-doubler rectifier with integrated magnetics," in *APEC. Seventeenth Annual IEEE Applied Power Electronics Conference and Exposition (Cat. No.02CH37335),* 2002, pp. 831-837, vol.2.

[62] W. Chen, G. Hua, D. Sable, and F. Lee, "Design of high efficiency, low profile, low voltage converter with integrated magnetics," in *Applied Power Electronics Conference and Exposition, 1997. APEC '97 Conference Proceedings 1997., Twelfth Annual*, 1997, pp. 911-917, vol.2.

[63] X. Peng, W. Qiaoqiao, W. Pit-Leong, and F. C. Lee, "A novel integrated current doubler rectifier," in *Applied Power Electronics Conference and Exposition, 2000. APEC 2000. Fifteenth Annual IEEE*, 2000, pp. 735-740, vol.2.

[64] X. Peng, Y. Mao, W. Pit-Leong, and F. C. Lee, "Design of 48 V voltage regulator modules with a novel integrated magnetics," *IEEE Transactions on Power Electronics*, vol. 17, no. 6, pp. 990-998, 2002.

[65] S. Jian, K. F. Webb, and V. Mehrotra, "Integrated magnetics for current-doubler rectifiers," *IEEE Transactions on Power Electronics,* vol. 19, no. 3, pp. 582-590, 2004.

[66] K. Jin, Z. Liu, X. Yu, and X. Ren, "A self-driven current-doubler-rectifier three-level converter with integrated magnetics," *IEEE Transactions on Power Electronics,* vol. 29, no. 7, pp. 3604-3615, 2014.

[67] S. Saggini, O. Zambetti, R. Rizzolatti, M. Picca, and P. Mattavelli, "An isolated quasi-resonant multi-phase single-stage topology for 48 V VRM applications," *IEEE Transactions on Power Electronics,* pp. 1-1, 2017.

[68] P. Zumel, O. Garcia, J. A. Cobos, and J. Uceda, "Magnetic integration for interleaved converters," in *Applied Power Electronics Conference and Exposition, 2003. APEC '03. Eighteenth Annual IEEE*, 2003, pp. 1143-1149, vol.2.

[69] N. H. Kutkut, "A full bridge soft switched telecom power supply with a current doubler rectifier," in *Proceedings of Power and Energy Systems in Converging Markets*, 1997, pp. 344-351.

[70] K. Kroics, J. Zakis, and U. Sirmelis, "Multiphase interleaved DC-DC converter with directly and inversely coupled inductors," in *2016 57th International Scientific Conference on Power and Electrical Engineering of Riga Technical University (RTUCON),* 2016, pp. 1-6.

[71] A. Pietkiewicz and D. Tollik, "Coupled-inductor current-doubler topology in phase-shifted full-bridge DC-DC converter," in *INTELEC–Twentieth International Telecommunications Energy Conference (Cat. No.98CH36263),* 1998, pp. 41-48.

[72] D. Yan, F. C. Lee, and X. Ming, "Evaluation of coupled inductor Voltage Regulators," in *2008 Twenty-Third Annual IEEE Applied Power Electronics Conference and Exposition,* 2008, pp. 831-837.

[73] Y. Dong, J. Zhou, F. C. Lee, M. Xu, and S. Wang, "Twisted core coupled inductors for microprocessor voltage regulators," *IEEE Transactions on Power Electronics*, vol. 23, no. 5, pp. 2536-2545, 2008.

[74] W. Huang and B. Lehman, " A compact coupled inductor for inter-

leaved multiphase DC–DC converters," *IEEE Transactions on Power Electronics,* vol. 31, no. 10, pp. 6770-6775, 2016.

[75] D. Huang, S. Ji, and F. C. Lee, "LLC resonant converter with matrix transformer," *IEEE Transactions on Power Electronics*, vol. 29, no. 8, pp. 4339-4347, 2014.

[76] M. H. Ahmed, C. Fei, F. C. Lee, and Q. Li, "48 V voltage regulator module with PCB winding matrix transformer for future data centers," *IEEE Transactions on Industrial Electronics*, vol. PP, no. 99, pp. 1-1, 2017.

[77] C. Fei, F. C. Lee, and Q. Li, "High-efficiency high-power-density LLC converter with an integrated planar matrix transformer for high output current applications," *IEEE Transactions on Industrial Electronics,* vol. PP, no. 99, pp. 1-1, 2017.

[78] C. Fei, Y. Yang, Q. Li, and F. C. Lee, "Shielding technique for planar matrix transformers to suppress common-mode EMI noise and improve efficiency," *IEEE Transactions on Industrial Electronics*, vol. 65, no. 2, pp. 1263-1272, 2018.

[79] L. Zhao, J. T. Strydom, and J. D. v. Wyk, "An integrated resonant module for a high power soft-switching converter," in *2001 IEEE 32nd Annual Power Electronics Specialists Conference (IEEE Cat. No.01CH37230),* 2001, pp. 1944-1948, vol. 4.

[80] C. Rengang, J. T. Strydom, and J. D. v. Wyk, "Design of planar integrated passive module for zero-voltage-switched asymmetrical half-bridge PWM converter," *IEEE Transactions on Industry Applications,* vol. 39, no. 6, pp. 1648-1655, 2003.

[81] C. Rengang, W. Shuo, J. D. v. Wyk, and W. G. Odendaal, "Integration of EMI filter for distributed power system (DPS) front-end converter," in *Power Electronics Specialist Conference, 2003. PESC '03. 2003 IEEE 34th Annual,* 2003, pp. 296-300, vol.1.

[82] C. Rengang, J. D. v. Wyk, S. Wang, and W. G. Odendaal, "Planar electromagnetic integration technologies for integrated EMI filters," in *38th IAS Annual Meeting on Conference Record of the Industry Applications Conference, 2003.*, 2003, pp. 1582-1588, vol.3.

[83] C. Rengang, J. D. v. Wyk, W. Shuo, and W. G. Odendaal, "Technologies and characteristics of integrated EMI filters for switch mode power supplies," in *2004 IEEE 35th Annual Power Electronics Specialists Conference (IEEE Cat. No.04CH37551)*, 2004, pp. 4873-4880, vol.6.

[84] M. C. Smit, J. A. Ferreira, and J. D. V. Wyk, "Application of transmission line principles to high frequency power converters," in *Power Electronics Specialists Conference, 1992. PESC '92 Record., 23rd Annual IEEE,* 1992, pp. 1423-1430, vol.2.

[85] M. Ehsani, O. H. Stielau, J. D. v. Wyk, and I. J. Pitel, "Integrated reactive components in power electronic circuits," *IEEE Transactions on Power Electronics*, vol. 8, no. 2, pp. 208-215, 1993.

[86] Z. Lingyin, J. T. Strydom, and J. D. v. Wyk, "A planar multicell structure for advanced integrated reactive power modules," *IEEE Transactions on Industry Applications,* vol. 39, no. 6, pp. 1656-1664, 2003.

[87] I. W. Hofsajer, J. A. Ferreira, and D. v. Wyk, "Design and analysis of planar integrated L-C-T components for converters," *IEEE Transactions on Power Electronics,* vol. 15, no. 6, pp. 1221-1227, 2000.

[88] J. T. Strydom, J. D. v. Wyk, and J. A. Ferreira, "Some limits of integrated L-C-T modules for resonant converters at 1 MHz," *IEEE Transactions on Industry Applications,* vol. 37, no. 3, pp. 820-828, 2001.

[89] P. A. J. V. Rensburg, J. D. V. Wyk, and J. A. Ferreira, "Design, prototyping and assessment of a 3 kW integrated LCT component for deployment in various resonant converters," *IET Power Electronics,* vol. 2, no. 5, pp. 535-544, 2009.

[90] M. C. Smit, J. A. Ferreira, J. D. V. Wyk, and M. Ehsani, "An ultrasonic series resonant converter with integrated L-C-T," *IEEE Transactions on Power Electronics,* vol. 10, no. 1, pp. 25-31, 1995.

[91] J. T. Strydom and J. D. v. Wyk, "Electromagnetic modeling for design and loss estimation of resonant integrated spiral planar power passives (ISP³)," *IEEE Transactions on Power Electronics,* vol. 19, no. 3, pp. 603-617, 2004.

[92] Z. Lingyin, J. T. Strydom, and J. D. v. Wyk, "Optimization and design of an integrated LC resonant module for medium and high power applications," in *2001 IEEE 32nd Annual Power Electronics Specialists Conference (IEEE Cat. No.01CH37230),* 2001, pp. 594-599, vol.2.

[93] J. T. Strydom and J. D. v. Wyk, "Volumetric limits of planar integrated resonant transformers: A 1 MHz case study," *IEEE Transactions on Power Electronics,* vol. 18, no. 1, pp. 236-247, 2003.

[94] Z. Lingyin and J. D. v. Wyk, "Wideband modeling of integrated power passive structures: The series resonator," *IEEE Transactions on Power Electronics,* vol. 19, no. 2, pp. 523-530, 2004.

[95] Z. Lingyin, J. T. Strydom, and J. D. v. Wyk, "Generalized frequency plane model of a spiral winding structure integrated power series resonator," *IEEE Transactions on Power Electronics*, vol. 20, no. 6, pp. 1254-1260, 2005.

[96] J. T. Strydom and J. D. v. Wyk, "Electromagnetic design optimization tool for resonant integrated spiral Planar Power passives (ISP<-sup>3</sup>)," *IEEE Transactions on Power Electronics,* vol. 20, no. 4, pp. 743-753, 2005.

[97] K. Lai-Dac, Y. Lembeye, A. Besri, and J. P. Keradec, "Analytical modeling of losses for high frequency planar LCT components," in *2009 IEEE Energy Conversion Congress and Exposition,* 2009, pp. 1883-1889.

[98] L. Seung-Yo, W. G. Odendaal, and J. D. v. Wyk, "Thermo-mechanical stress analysis for an integrated passive resonant module," *IEEE Transactions on Industry Applications,* vol. 40, no. 1, pp. 94-102, 2004.

[99] W. Liu, J. Dirker, and J. D. v. Wyk, "Power density improvement in integrated electromagnetic passive modules with embedded heat extractors," *IEEE Transactions on Power Electronics,* vol. 23, no. 6, pp. 3142-3150, 2008.

[100] L. Wenduo and J. D. v. Wyk, "Design of integrated LLCT module for LLC resonant converter," in *Twentieth Annual IEEE Applied Power Electronics Conference and Exposition, 2005. APEC 2005*., 2005, pp. 362-368, vol. 1.

[101] E. Waffenschmidt and J. A. Ferreira, "Embedded passives integrated circuits for power converters," in *2002 IEEE 33rd Annual IEEE Power Electronics Specialists Conference. Proceedings (Cat. No.02CH37289),* 2002, pp. 12-17, vol.1.

[102] E. Waffenschmidt, B. Ackermann, and J. A. Ferreira, "Design method and material technologies for passives in printed circuit Board Embedded circuits," *IEEE Transactions on Power Electronics,* vol. 20, no. 3, pp. 576-584, 2005.

[103] Q. Chen, Z. Gong, X. Yang, Z. Wang, and L. Zhang, "Design considerations for passive substrate with ferrite materials embedded in printed circuit board (PCB)," in *2007 IEEE Power Electronics Specialists Conference,* 2007, pp. 1043-1047.

[104] Z. Gong, Q. Chen, X. Yang, B. Yuan, W. Feng, and Z. Wang, "Design of high power density DC-DC converter based on embedded passive substrate," in *2008 IEEE Power Electronics Specialists Conference,* 2008, pp. 273-277.

[105] R. Meere, T. O. Donnell, H. J. Bergveld, N. Wang, and S. C. O. Mathuna, "Analysis of microinductor performance in a 20–100 MHz DC/DC converter," *IEEE Trans. Power Electron.,* vol. 24, no. 9, pp. 2212-2218, Sept. 2009.

[106] D. Disney and Z. J. Shen, "Review of silicon power semiconductor technologies for power supply on chip and power supply in package applications," *IEEE Trans. Power Electron.,* vol. 28, no. 9, pp. 4168-4181, Sept. 2013.

[107] C. Ó. Mathúna, N. Wang, S. Kulkarni, and S. Roy, "Review of integrated magnetics for power supply on chip (PwrSoC)," *IEEE Trans. Power Electron.,* vol. 27, no. 11, pp. 4799-4816, Nov. 2012.

[108] T. O. Donnell, N. Wang, R. Meere, F. Rhen, S. Roy, D. O. Sullivan et al., "Microfabricated inductors for 20 MHz Dc-Dc converters," in *2008 Twenty-Third Annual IEEE Applied Power Electronics Conference and Exposition,* 2008, pp. 689-693.

[109] R. Meere, N. Wang, T. O. Donnell, S. Kulkarni, S. Roy, and S. C. O. Mathuna, "Magnetic-core and air-core inductors on silicon: A performance comparison up to 100 MHz," *IEEE Transactions on Magnetics*, vol. 47, no. 10, pp. 4429-4432, Oct. 2011.

[110] P. Dhagat, S. Prabhakaran, and C. R. Sullivan, "Comparison of magnetic materials for V-groove inductors in optimized high-frequency DC-DC converters," *IEEE Transactions on Magnetics*, vol. 40, no. 4, pp. 2008-2010, July 2004.

[111] D. Yao, C. G. Levey, R. Tian, and C. R. Sullivan, "Microfabricated V-groove power inductors using multilayer Co-Zr-O thin films for

very-high-frequency DC-DC converters," *IEEE Trans. Power Electron.,* vol. 28, no. 9, pp. 4384-4394, Sept. 2013.

[112] M. Lee, Y. Choi, and J. Kim, "A 500-MHz, 0.76-W/mm power density and 76.2% power efficiency, fully integrated digital buck converter in 65-nm CMOS," *IEEE Trans. Ind. Applicat*., vol. 52, no. 4, pp. 3315-3323, July-Aug. 2016.

[113] L. Wang, W. Liu, D. Malcolm, and Y. F. Liu, "An integrated power module based on power-system-in-inductor structure," *IEEE Trans. Power Electron.,* vol. PP, no. 99, pp. 1-1, 2017.

[114] L. Wang, D. Malcolm, and Y. F. Liu, "An innovative power module with power-system-in-inductor structure," in *2016 IEEE Applied Power Electronics Conference and Exposition (APEC)*, 2016, pp. 2087-2094.

[115] F. C. Lee and Q. Li, "High-frequency integrated point-of-load converters: Overview," *IEEE Trans. Power Electron.*, vol. 28, no. 9, pp. 4127-4136, Sept. 2013.

[116] W. Zhang, Y. Su, M. Mu, D. J. Gilham, Q. Li, and F. C. Lee, "High-density integration of high-frequency high-current point-of-load (POL) modules with planar inductors," *IEEE Trans. Power Electron.,* vol. 30, no. 3, pp. 1421-1431, Mar. 2015.

[117] S. Ji, D. Reusch, and F. C. Lee, "High-frequency high power density 3-D integrated gallium-nitride-based point of load module design," *IEEE Trans. Power Electron.,* vol. 28, no. 9, pp. 4216-4226, Sept. 2013.

[118] L. Wang, Y. Pei, B. S. X. Yang, Z. Wang, and G. Zhao, "Evaluation of LTCC capacitors and inductors in DC/DC converters," in *2010 Twenty-Fifth Annual IEEE Applied Power Electronics Conference and Exposition (APEC),* 2010, pp. 2060-2065.

[119] L. Wang, Y. Pei, X. Yang, X. Cui, and Z. Wang, "Three-dimensional integration of high frequency DC/DC converters based on LTCC technology," in *2009 IEEE 6th International Power Electronics and Motion Control Conference,* 2009, pp. 745-748.

[120] L. Wang, Y. Pei, X. Yang, and Z. Wang, "Design of ultrathin LTCC coupled inductors for compact DC/DC converters," *IEEE Trans. Power Electron.,* vol. 26, no. 9, pp. 2528-2541, Sept. 2011.

[121] L. Wang, Y. Pei, X. Yang, X. Cui, Z. Wang, and G. Zhao, "A class of coupled inductors based on LTCC technology," *in 2010 Twenty-Fifth Annual IEEE Applied Power Electronics Conference and Exposition (APEC),* 2010, pp. 2042-2049.

[122] L. Wang, Z. Hu, Y. F. Liu, Y. Pei, and X. Yang, "Multipermeability inductors for increasing the inductance and improving the efficiency of high-frequency DC/DC converters," *IEEE Trans. Power Electron.,* vol. 28, no. 9, pp. 4402-4413, Sept. 2013.

[123] L. Wang, Z. Hu, Y. F. Liu, Y. Pei, X. Yang, and Z. Wang, "A horizontal-winding multipermeability LTCC inductor for a low-profile hybrid DC/DC converter," *IEEE Trans. Power Electron*., vol. 28, no. 9, pp. 4365-4375, Sept. 2013.

[124] L. Wang, Z. Hu, Y. f. Liu, Y. Pei, and X. Yang, "Design of multi-permeability distributed air-gap inductors," *in 2012 IEEE Energy Conversion Congress and Exposition (ECCE),* 2012, pp. 3285-3292.

[125] L. Wang, Y. Pei, X. Yang, Y. Qin, and Z. Wang, "Improving light and intermediate load efficiencies of buck converters with planar nonlinear inductors and variable on time control," *IEEE Trans. Power Electron.,* vol. 27, no. 1, pp. 342-353, Jan. 2012.

[126] L. Wang, Y. Pei, X. Yang, and Z. Wang, "Improving light load efficiency of high frequency DC/DC converters with planar nonlinear inductors," in *2010 IEEE Energy Conversion Congress and Exposition,* 2010, pp. 2237-2244.

[127] L. Wang, Y. Qiu, H. Wang, Z. Hu, and Y. F. Liu, "A new model for designing multiwindow multipermeability nonlinear LTCC inductors," *IEEE Trans. Ind. Applicat.*, vol. 51, no. 6, pp. 4677-4687, Nov.-Dec. 2015.

[128] M. H. Lim, J. D. v. Wyk, F. C. Lee, and K. D. T. Ngo, "A class of ceramic-based chip inductors for hybrid integration in power supplies," *IEEE Trans. Power Electron*., vol. 23, no. 3, pp. 1556-1564, May 2008.

[129] Y. Su, Q. Li, and F. C. Lee, "Design and evaluation of a high-frequency LTCC inductor substrate for a three-dimensional integrated DC/DC converter," *IEEE Trans. Power Electron.*, vol. 28, no. 9, pp. 4354-4364, Sept. 2013.

[130] Q. Li, Y. Dong, and F. C. Lee, "High density low profile coupled inductor design for integrated point-of-load converter," *in 2010 Twenty-Fifth Annual IEEE Applied Power Electronics Conference and Exposition (APEC),* 2010, pp. 79-85.

[131] S. Ji, D. Reusch, and F. C. Lee, "High frequency high power density 3D integrated Gallium Nitride based point of load module," *in 2012 IEEE Energy Conversion Congress and Exposition (ECCE)*, 2012, pp. 4267-4273.

[132] Q. Li, Y. Dong, F. C. Lee, and D. J. Gilham, "High-density low-profile coupled inductor design for integrated point-of-load converters," *IEEE Trans. Power Electron*., vol. 28, no. 1, pp. 547-554, Jan. 2013.

[133] M. H. F. Lim, J. D. v. Wyk, and F. C. Lee, "Hybrid integration of a low-voltage, high-current power supply buck converter with an LTCC substrate inductor," *IEEE Trans. Power Electron.*, vol. 25, no. 9, pp. 2287-2298, Sept. 2010.

[134] M. Mu, W. Zhang, F. C. Lee, and Y. Su, "Laminated low temperature co-fired ceramic ferrite materials and the applications for high current POL converters," in *2013 IEEE Energy Conversion Congress and Exposition,* 2013, pp. 621-627.

[135] Y. Su, Q. Li, M. Mu, D. Gilham, D. Reusch, and F. C. Lee, "Low profile LTCC inductor substrate for multi-MHz integrated POL converter," in *2012 Twenty-Seventh Annual IEEE Applied Power Electronics Conference and Exposition (APEC),* 2012, pp. 1331-1337.

[136] Q. Li, Y. Su, M. Mu, F. C. Lee, and D. Gilham, "Modeling of planar inductors with non-uniform flux distribution and non-linear permeability for high-density integration," in *2012 Twenty-Seventh Annual IEEE Applied Power Electronics Conference and Exposition (APEC),* 2012, pp. 1002-1009.

[137] M. Mu, Y. Su, Q. Li, and F. C. Lee, "Magnetic characterization of low temperature co-fired ceramic (LTCC) ferrite materials for high frequency power converters," in *2011 IEEE Energy Conversion Congress and Exposition,* 2011, pp. 2133-2138.

[138] M. Mu, F. Zheng, Q. Li, and F. C. Lee, "Finite element analysis of inductor core loss under DC bias condition," in *2012 Twenty-Seventh Annual IEEE Applied Power Electronics Conference and Exposition (APEC),* 2012, pp. 405-410.

[139] Q. Li, M. Mu, and F. C. Lee, "Analytical core loss models for planar inductors with non-uniform flux distribution and non-sinusoidal excitation," in *2012 Twenty-Seventh Annual IEEE Applied Power Electronics Conference and Exposition (APEC),* 2012, pp. 1783-1789.

Kangping Wang was born in Shaanxi, China, in 1989. He received the B.S. degree in electrical engineering from Xi'an Jiaotong University, Xi'an, China, in 2012. He is currently pursuing the Ph.D. degree in electrical engineering at Xi'an Jiaotong University. From August 2016 to August 2017, he was with the Department of ePOWER, Electrical and Computer Engineering, Queen's University, Kingston, ON, Canada, as a joint Ph.D. student.

His research interests include high-frequency power converters and wide bandgap devices.

Zhiyuan Qi was born in Henan, China, in 1989. He received the B.S. and M.S. degree in electrical engineering and automation in 2012 and 2015, respectively, from Harbin Engineering University, Harbin, China. He is currently working toward the Ph.D. degree in electrical engineering at Xi'an Jiaotong University.

His research interests include power electronic integration and high-frequency power conversion technologies.

Fei Li was born in Shaanxi, China, in 1992. She received the B.S. degree in electrical engineering from Xi'an Jiaotong University, Xi'an, China, in 2014. She is currently working toward the Ph.D. degree in electrical engineering at Xi'an Jiaotong University.

Her research interests include magnetic integration and low-voltage high-current conversion technique.

Laili Wang was born in Shaanxi province, China, in 1982. He received the B.S., M.S. and Ph.D. degrees in electrical engineering from Xi'an Jiaotong University, Xi'an, China, in 2004, 2007 and 2011 respectively. Since 2011, he has been a Postdoctoral Research Fellow in the electrical engineering department, Queen's University, Canada. From 2014 to 2017, he was an electrical engineer in Sumida, Canada. In 2017, he joined in Xi'an Jiaotong University as a professor.

His research focuses on package and integration of passive devices in high frequency high power density dc/dc converters.

Xu Yang received the B.S. and Ph.D. degrees in electrical engineering from Xi'an Jiaotong University, Xi'an, China, in 1994 and 1999, respectively.

Since 1999, he has been a member of the faculty of School of Electrical Engineering, Xi'an Jiaotong University, where he is presently a professor. From November 2004 to November 2005, he was with the Center of Power Electronics Systems (CPES), Virginia Polytechnic Institute and State University, Blacksburg, VA, as a Visiting Scholar. He then came back to Xi'an Jiaotong University, and engaged in the teaching and researches in power electronics and industrial automation area.

His research interests include soft switching topologies, PWM control techniques and power electronic integration, and packaging technologies.